New Structure for Adder with Improved Speed, Area and Power

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- Two main Adder structures
  - Ripple Carry Adder
  - Carry Look ahead Adder
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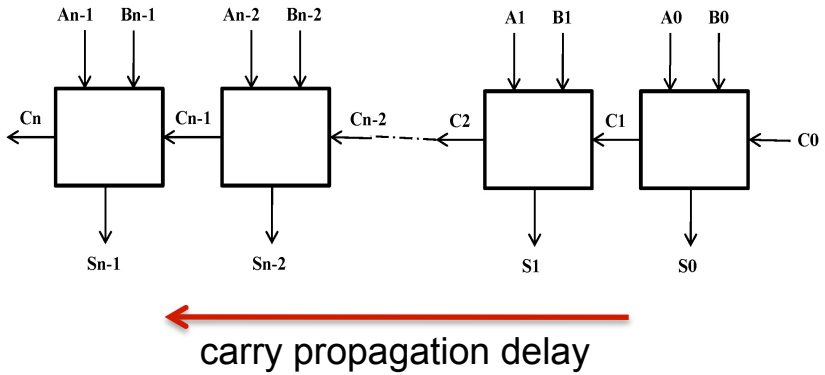
Ripple Carry Adder

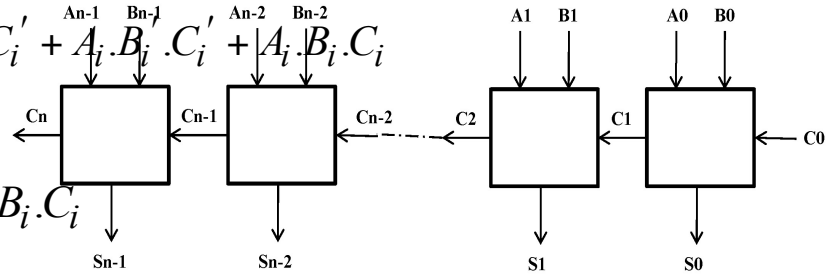
- The Ripple Carry Adder (RCA) :
  - Based on mathematical calculations by hand
  - The simplest adder
  - Cascading full adder blocks
  - Occupies large on-chip area



Ripple Carry Adder

$$S_i = A_i'.B_i'.C_i + A_i'.B_i.C_i' + A_i.B_i'.C_i' + A_i.B_i.C_i$$
$$= A_i \oplus B_i \oplus C_i$$

$$C_{i+1} = A_i.B_i + A_i.C_i + B_i.C_i$$



carry propagation delay

Adders

- Maximum delay of adders is due to generation of carry signals

Some Solutions ⇩

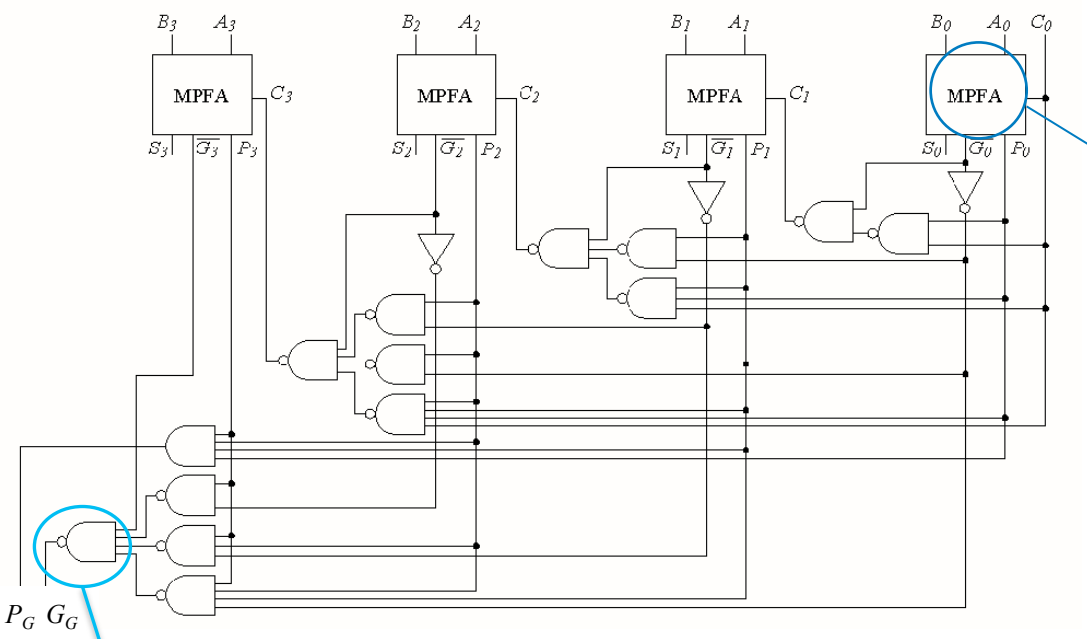
Carry Select Adder(CSA) , Carry Skip Adder & Carry Look-ahead Adder (CLA)

⇩	⇩	⇩
Faster but its area is 2 times larger than RCA	Slower than CSA but smaller area	Very Faster than others with very larger area because of LCUs

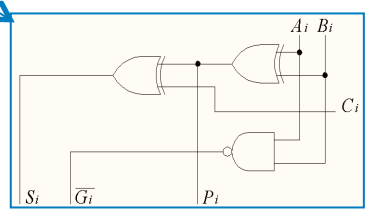
There is a trade off between speed and area

proposed structure: Decreasing the area and power while preserving the speed

Carry Look-ahead Adder



Simplified Carry Look ahead Adder (SpCLA)



Metamorphosis of Partial Full Adder

$$P_i = A_i \oplus B_i \quad : \quad Propagate\,Signal$$

$$G_i = A_i \cdot B_i \quad : \quad Generate\,Signal$$

P & G signals for look-ahead carries

Replaced with AND gate: modified Carry Look ahead Adder (MCLA) [11]

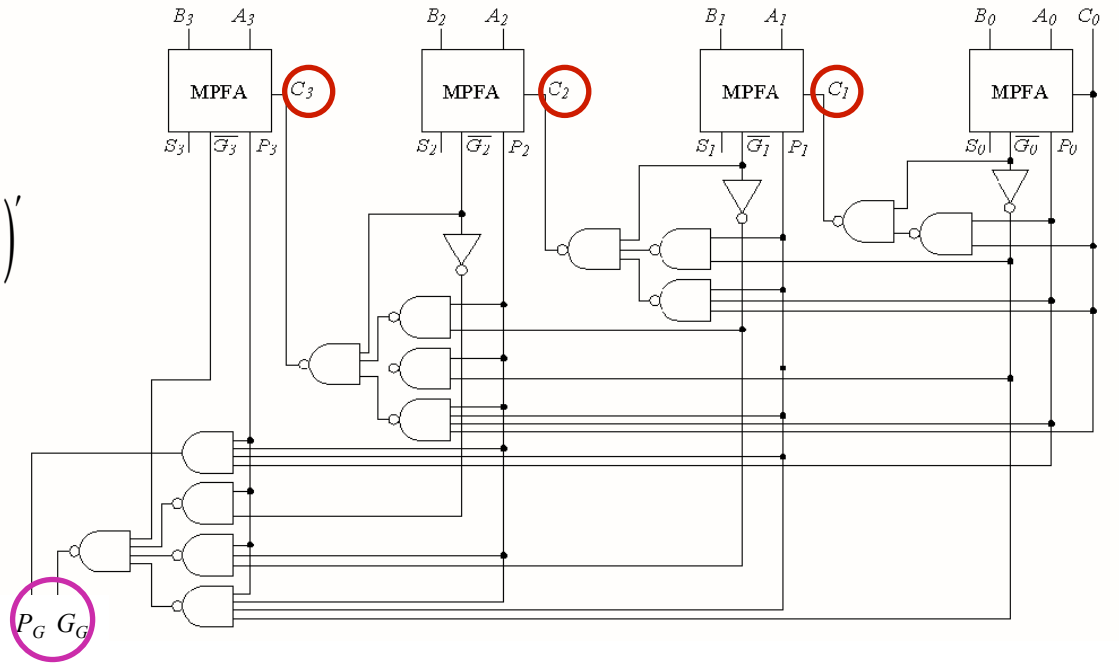
Carry Look-ahead Adder

$$C_1 = \left(G_0'.\left(P_0.C_0\right)' \right)'$$

$$C_2 = \left(G_1'.\left(P_1.G_0\right)'.\left(P_1.P_0.C_0\right)' \right)'$$

$$C_3 = \left(G_2'.\left(P_2.G_1\right)'.\left(P_2.P_1.G_0\right)'.\left(P_2.P_1.P_0.C_0\right)' \right)'$$

$$C_4 = \left(\begin{array}{c} G_3.\left(P_3.G_2\right)'.\left(P_3.P_2.G_1\right)'. \\ \left(P_3.P_2.P_1.G_0\right)'.\left(P_3.P_2.P_1.P_0.C_0\right)' \end{array} \right)'$$



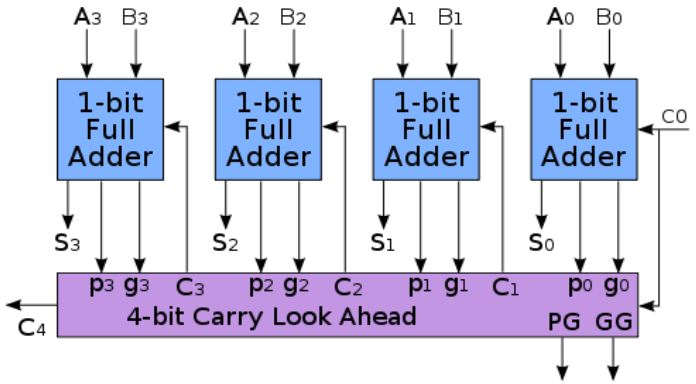
$$P_G = P_3.P_2.P_1.P_0$$

$$G_G = G_3 + P_3.G_2 + P_3.P_2.G_1 + P_3.P_2.P_1.G_0$$

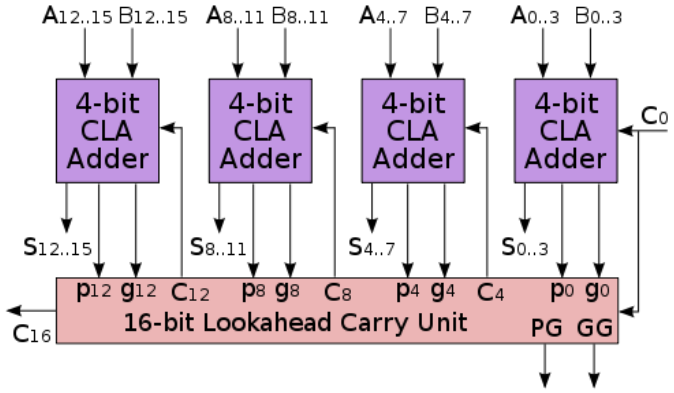
$$C_4 = G_G + P_G.C_0$$

The carry logic is getting quite complicated for more than 4 bits

Carry Look-ahead Adder

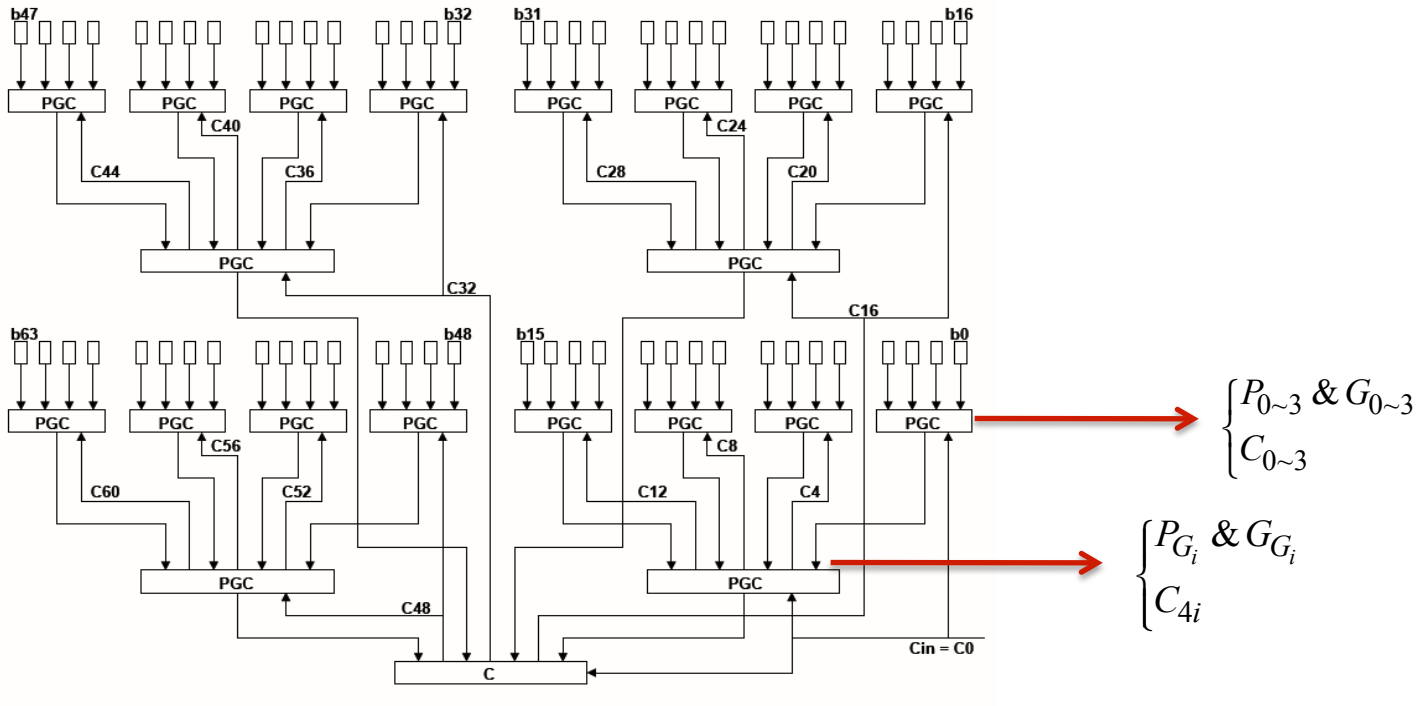


By combining four 4-bit CLAs, a 16-bit adder can be created



By combining four 16-bit CLAs, a 64-bit adder can be created

64- Bit CLA



64-Bit CLA structure

Proposed Structure

- Only C_{4i} are predicted in PGC blocks with P & G signals.
- Other carries are generated similar to Ripple Carry Adder.

⇒ Reduction loading on the P and G signals in each LCUs

⇓

faster production of P_G & G_G signals ⇒ Speed up of C_{4i} & S_i

So our proposed adder structure has been named *RCLA*

(Ripple Carry Look-ahead Adder)

- Advantages of this new structure:

On-chip area ↓ & Delay ↓ & Power consumption ↓

It's very good !

Simulation Results

- Simulated with HSPICE , TSMC 0.18μm CMOS technology , 1.8v power supply
- Critical path: the path of S_{63} signal generation

comparison of delay in MCLA and proposed structure:

			Original MCLA	*Proposed Structure*
delay	S_{63}	*Rising Edge*	2.19 ns	2.02 ns
		Falling Edge	2.094 ns	1.894 ns
	C_{64}	*Rising Edge*	0.957 ns	0.915 ns
		Falling Edge	0.795 ns	0.752 ns
d= Maximum Delay			2.19 ns	2.02 ns **(7.8% decrease)**

Simulation Results

comparison of power consumption in MCLA to that in the proposed structures:

	Original MCLA	*Proposed Structure*
N= Total number of transistors	*4288*	3872 ***(10% decrease(***
P_{ave} ***(mw)***	*0.435*	0.426 ***(2.1% decrease)***

Simulation Results

β: Comparison both parameters, speed and area, simultaneously

γ: Comparison all three parameters delay, total number of transistors and Power consumption:

	Original MCLA	*Proposed Structure*
$\beta = d \times N$	*9391*	*7820*
$\gamma = d \times N \times P_{ave}$	*4085*	*3332*

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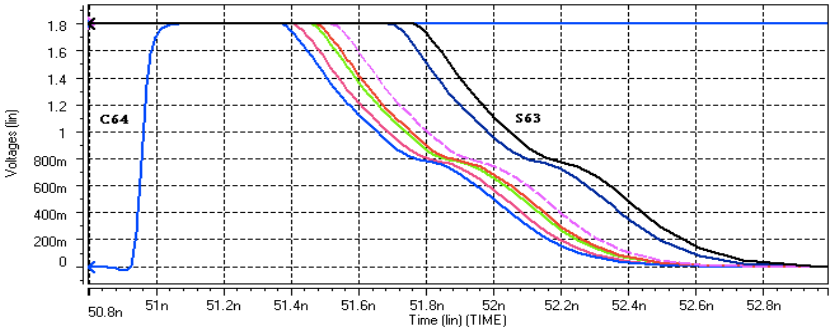
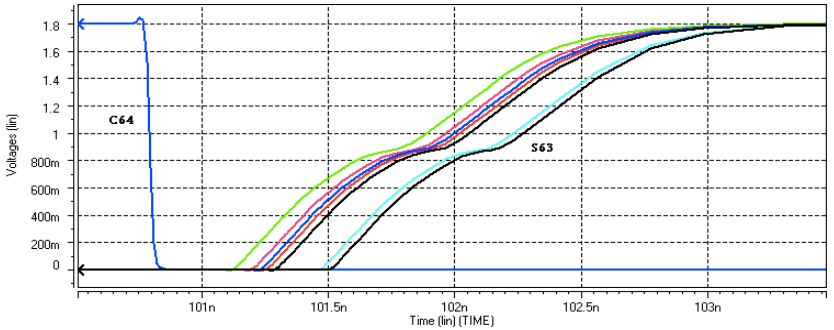
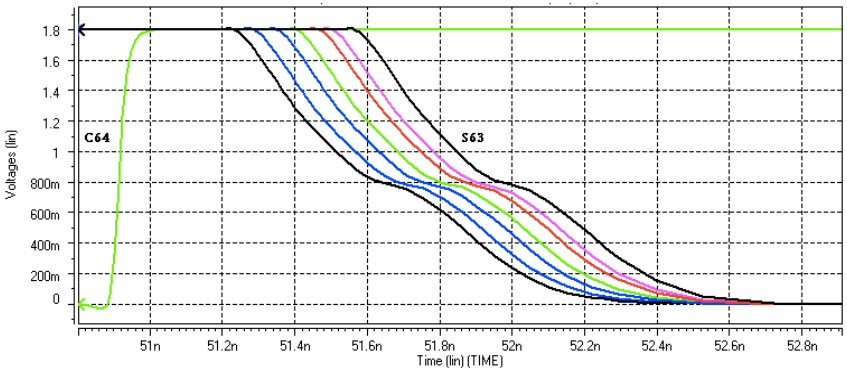
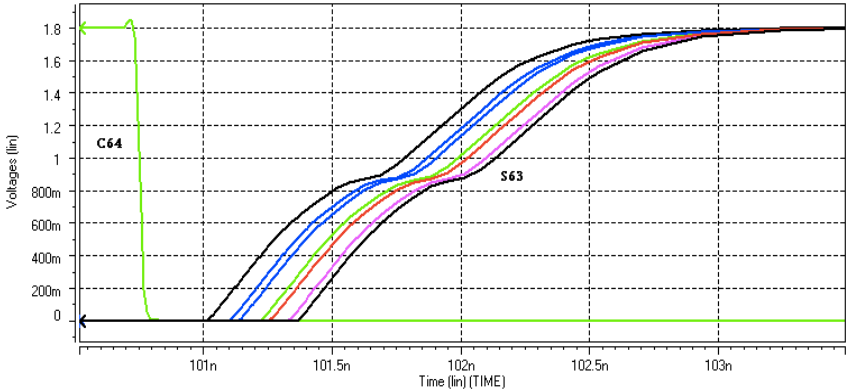




Wave forms of the summation and carry out (S_{57}~S_{63} and C_{64}) of MCLA structure in two states, rising and falling edges. As it is shown, compared to the other outputs in worst case condition, S_{63} signal has maximum delay in rising edge. Therefore the total delay of MCLA is related to it.





Wave forms of the summation and carry out (S_{57}~S_{63} and C_{64}) of proposed structure in two states, rising and falling edges. As it is shown, compared to the other outputs in worst case condition, S_{63} signal has maximum delay in rising edge. Therefore the total delay of new structure is related to it.