A Study on Accelerated Built-in Self Test of Multi-Gb/s High Speed Interfaces

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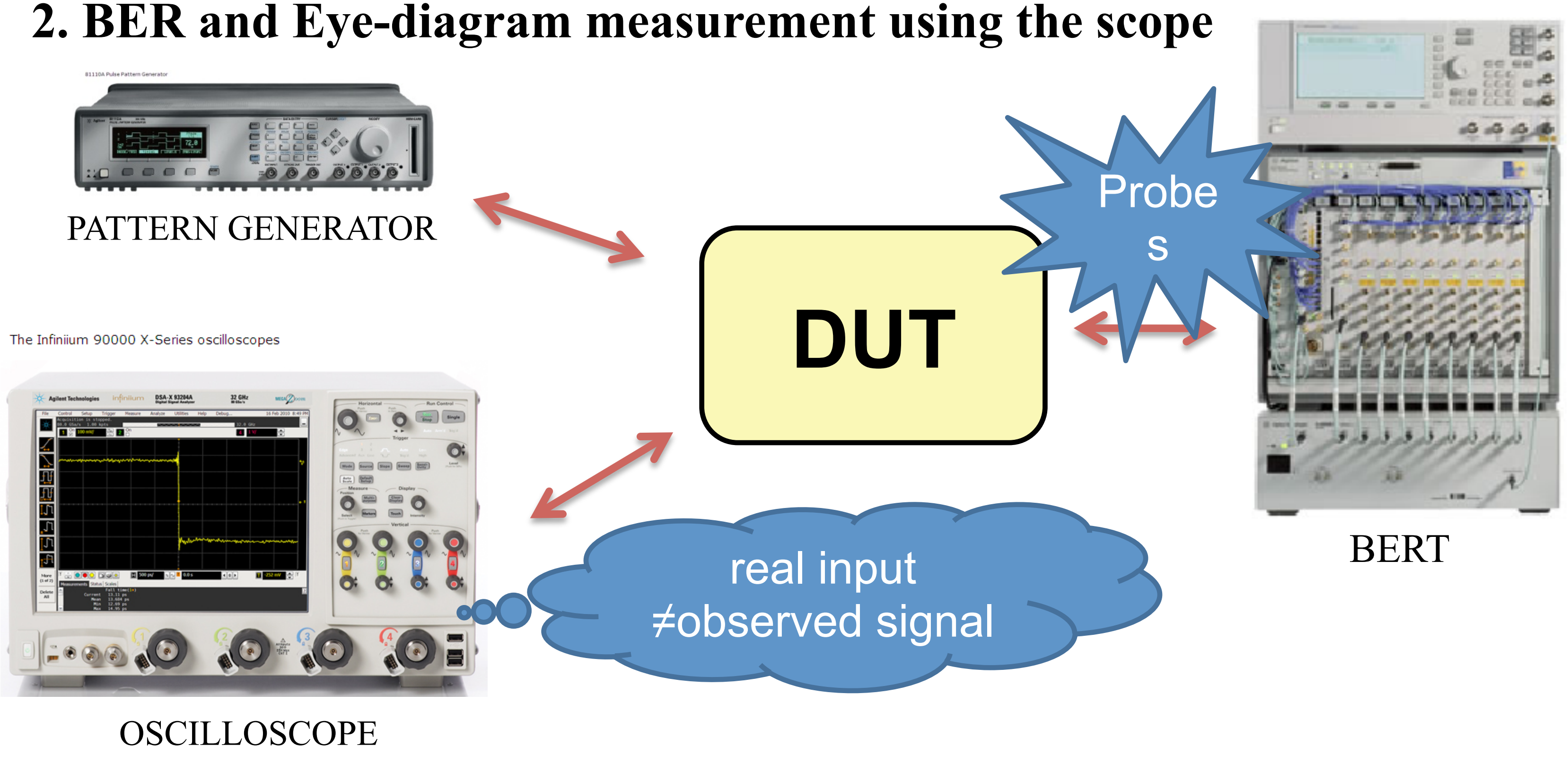
1. Introduction

1. Noise budgeting and Noise immunity

Important factor to analysis the performance of the high speed serial interfaces.

2. BER and Eye-diagram measurement using the scope



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1. Test architecture

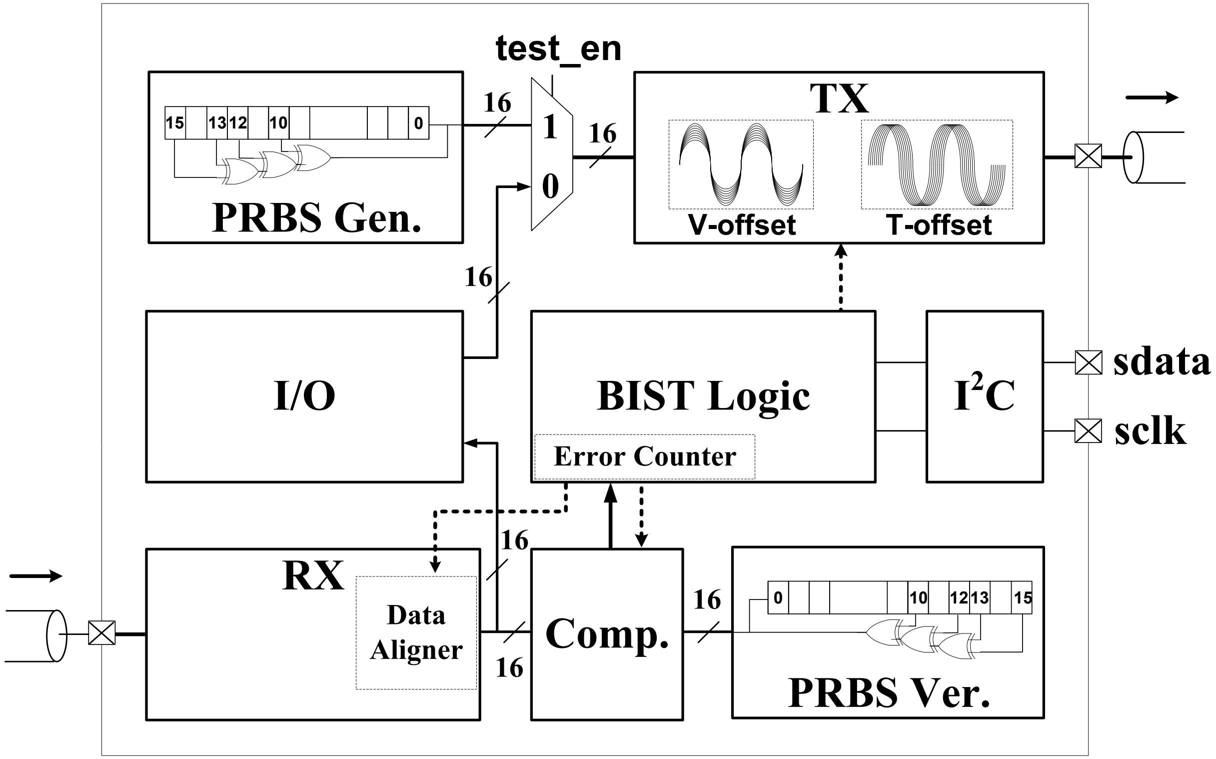
1. Proposed BIST architecture

I2C interface

Tx with offset controllers, Rx with data aligner

PRBS generator, PRBS verifier

BIST logic with a bit error counter and a comparator



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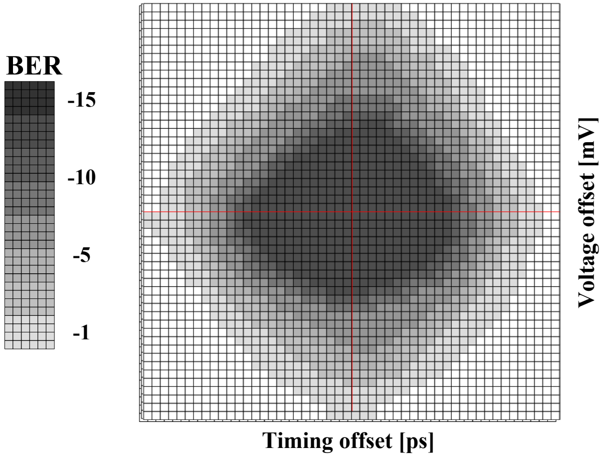
3. Stereographic BER test

1. Stereographic BER test sequence

Intentionally generate timing offset (Δt) voltage offset (ΔV)



- Starts from the center of timing offset-axis
- BER measurement is repeated over all the voltage offset values
- BER test rerun with the next timing offset along all the voltage offset range
- BER data is collected over all points in the Δt-ΔV plane
- Color codes are assigned according to BER level
- A full 2-dimensional stereographic BER diagram

→ Visualize the timing and voltage margins of the interface circuit under test

10^{-15} @ 1Gbps 10^{6} seconds

10^{-6} @ 4.8Gbs 0.2 m seconds

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5. Accelerated test
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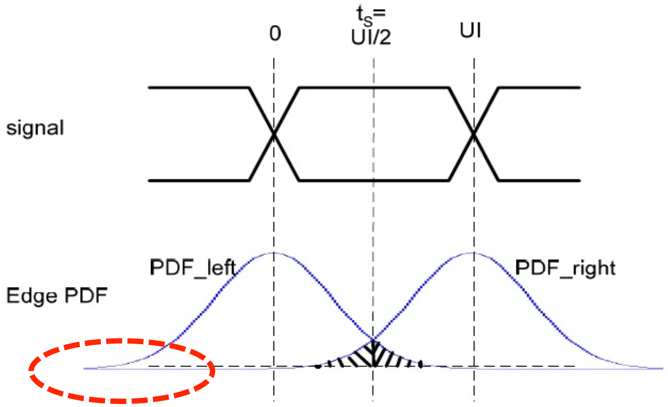
4. BER modeling

1. Relationship between data sampling points and PDF

Ideally, the data are always sampled in the mid-bit.

For out-of -band jitter cause bit errors

Example of the jitter profile



Distributed by Random jitter

Signal edge transition is distributed by RJ

RJ is assumed to be Gaussian

4. BER modeling

2. BER modeling

The probability density function of a zero-mean Gaussian variable is

$$p(x) = \frac{1}{\delta\sqrt{2\pi}} e^{-\frac{x^2}{2\delta^2}}$$

where σ is the standard deviation.

Assuming the uniform bit distribution, the BER can be expressed

(the probability of bit transition is 50% when each error occurs)

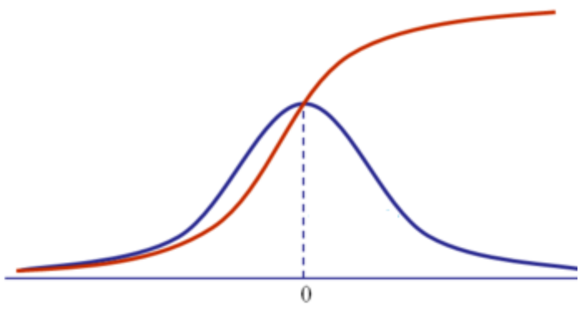
$$BER = 0.5*\left(\int_{\Delta t}^{\infty} P\_left(t)dt + \int_{-\infty}^{\Delta t} P\_right(t)dt\right)$$

$$= 0.5*\left(\int_{\Delta t}^{\infty} \frac{1}{\delta\sqrt{2\pi}} e^{-\frac{t^2}{2\delta^2}} dt + \int_{-\infty}^{\Delta t} \frac{1}{\delta\sqrt{2\pi}} e^{-\frac{(t-UI)^2}{2\delta^2}} dt\right)$$

$$= \int_{\Delta t}^{\infty} \frac{1}{\delta\sqrt{2\pi}} e^{-\frac{t^2}{2\delta^2}} dt$$

4. BER modeling

Integral of the Gaussian function turns into complementary error function.



CDF
(Cumulative distribution function)
for the Gaussian distributions

Gaussian distributions

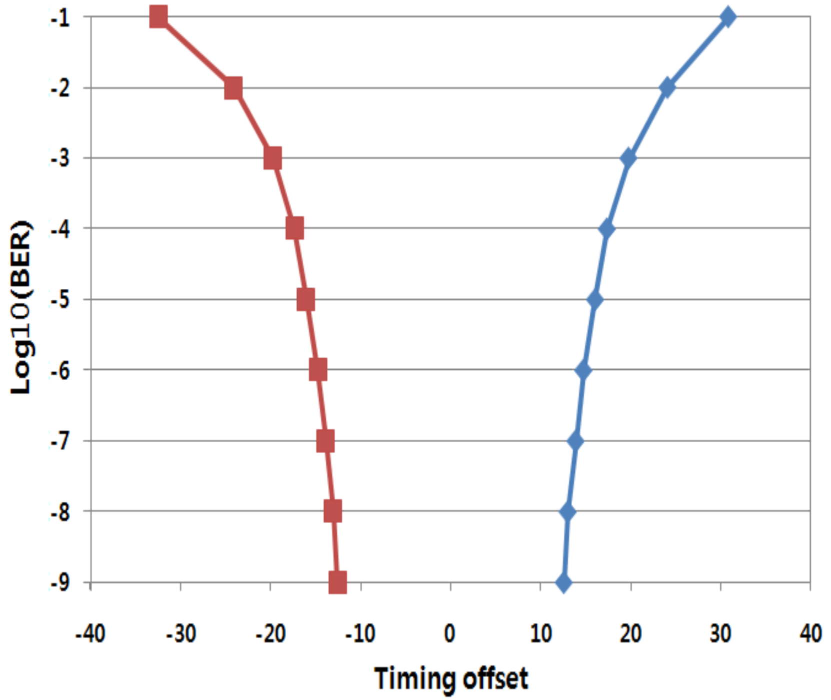
Complementary error function can be approximated to another Gaussian function for small Δt/ σ

Simplified equation is

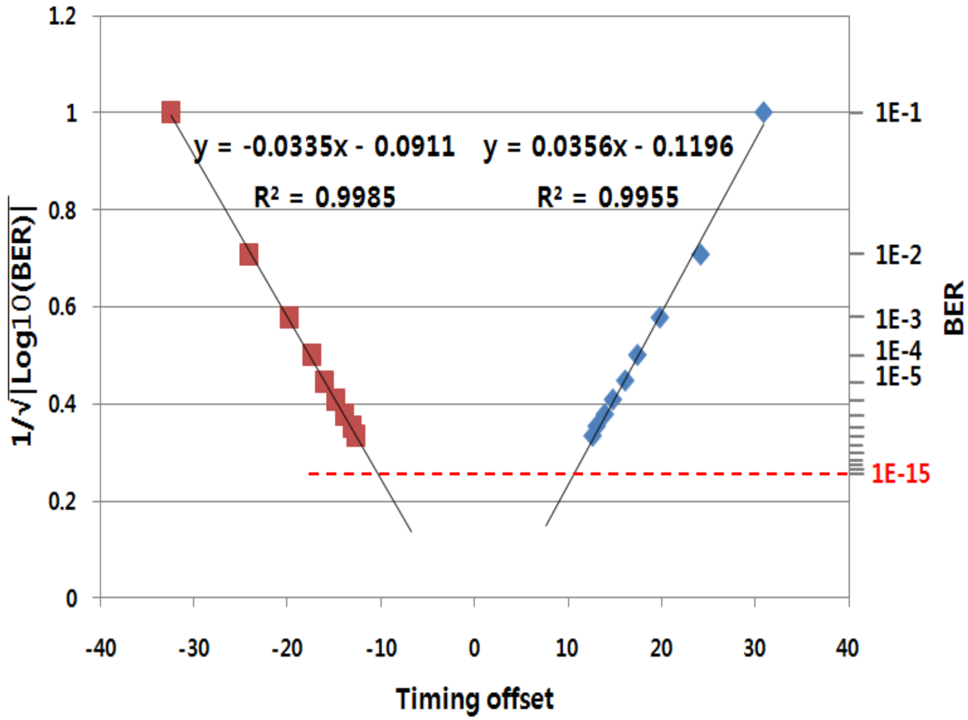
$$|Log_{10}(BER)| = \frac{A}{(\Delta t)^2} + B$$

where both A and B are constants.

4. BER modeling

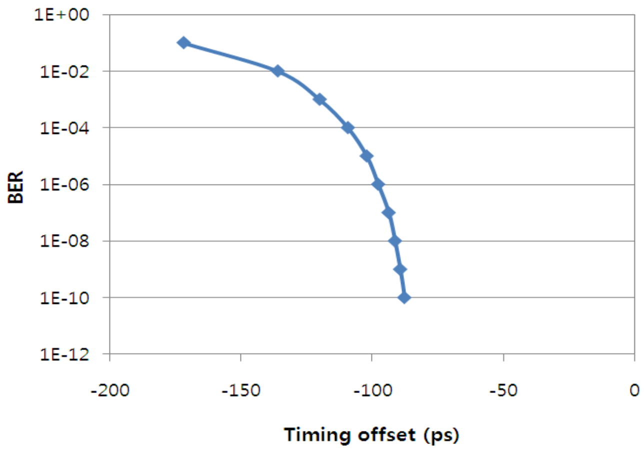


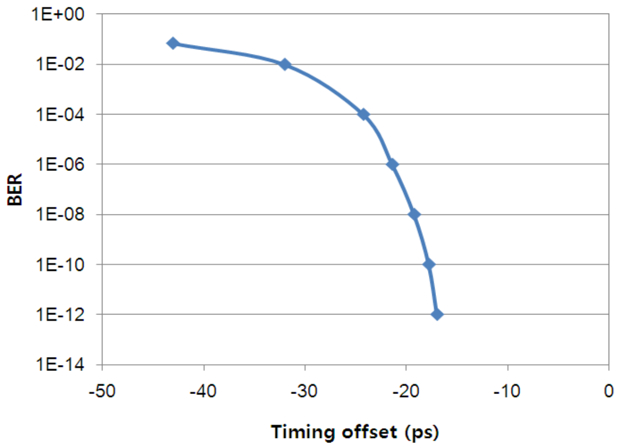
Cross-section view of the stereographic BER diagram

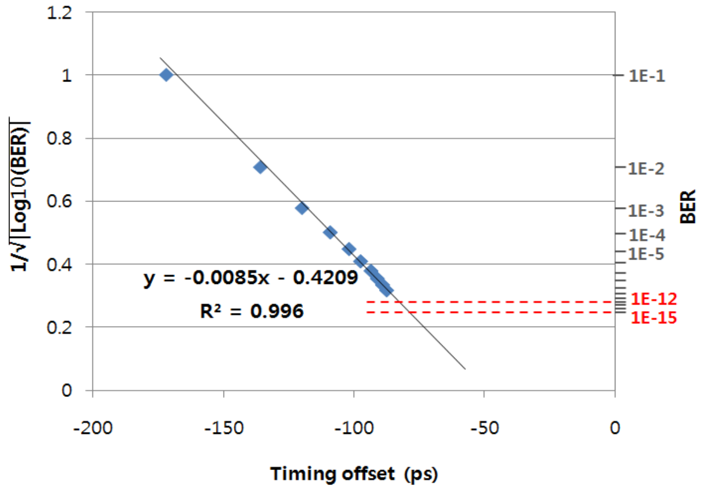


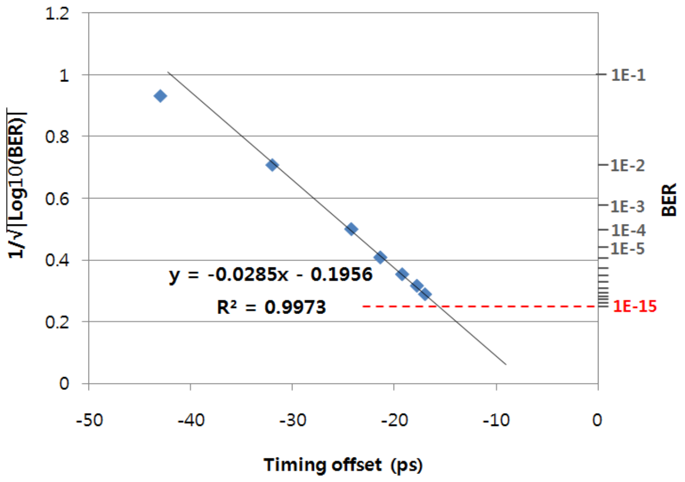
Curve fitting of the timing offset and BER

4. BER modeling









[6] LVDS Owner's Manual, Fourth Edition, national.com/LVDS, pp.58, Fig. 6-13, 2008.

[7] Michael Nelson, Pavel Zivny, "Impact of Noise on BER estimation", Tektronix, August 2005.

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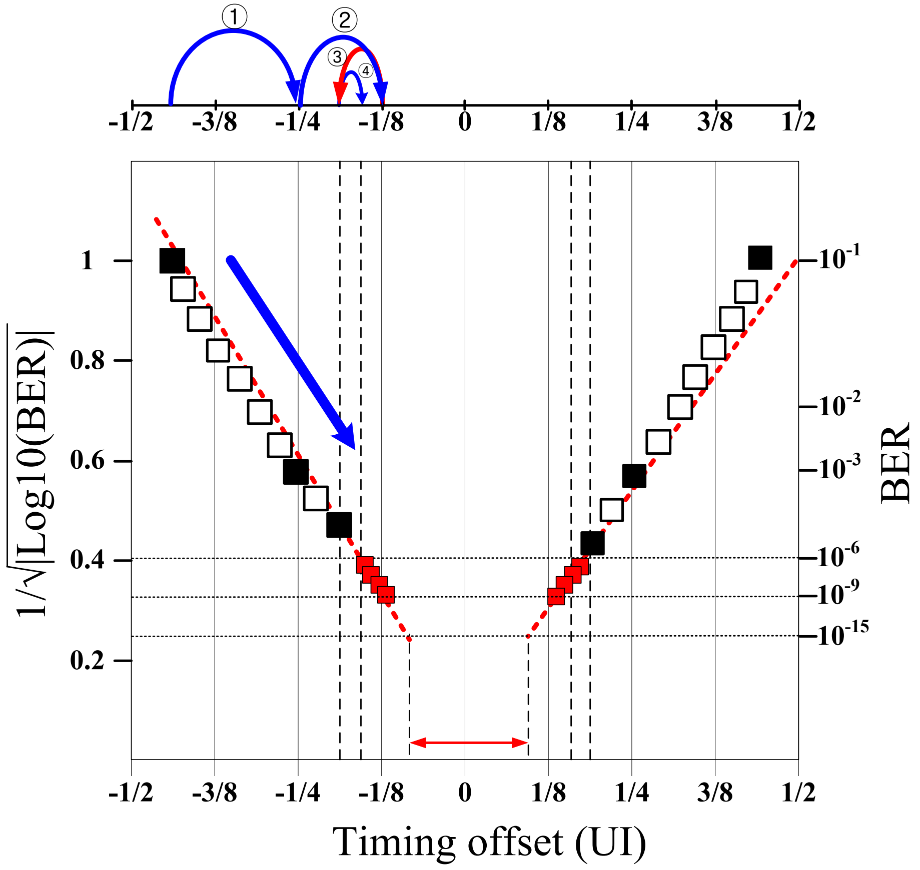
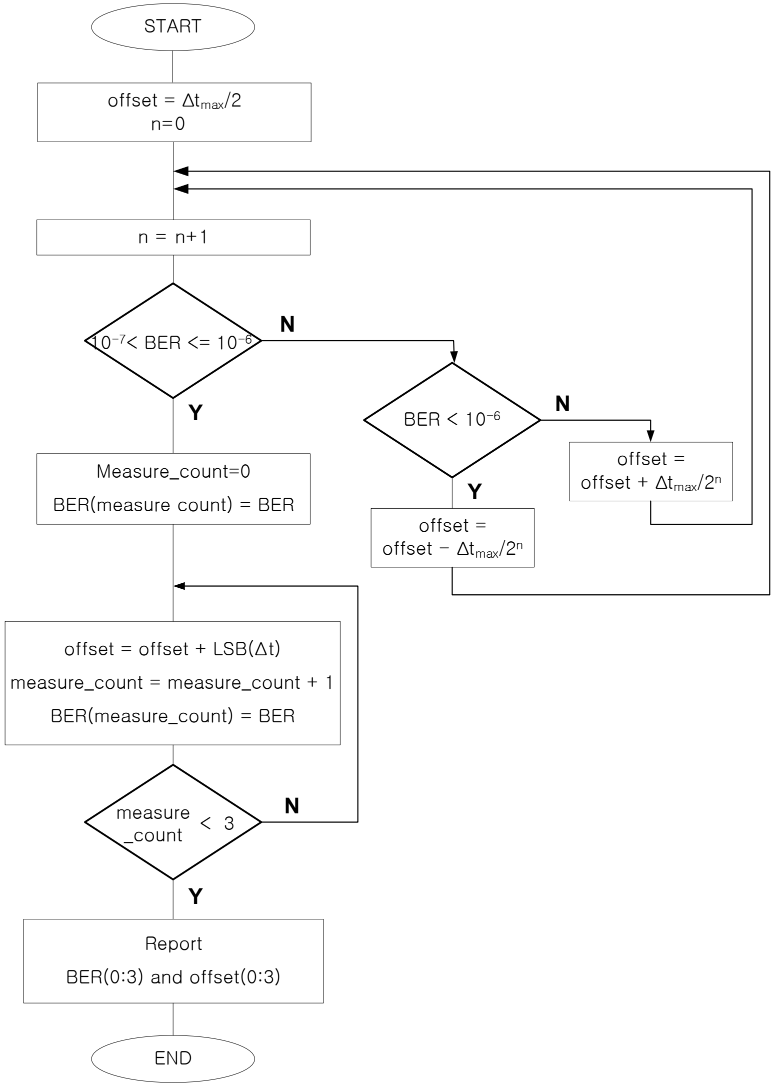
5. Accelerated test





START

offset = $\Delta t_{max}/2$
n=0

n = n+1

10^{-7} < BER <= 10^{-6}

N

Y

Measure_count=0

BER(measure count) = BER

BER < 10^{-6}

N

offset = offset + $\Delta t_{max}/2^n$

Y

offset = offset − $\Delta t_{max}/2^n$

offset = offset + LSB(Δt)

measure_count = measure_count + 1

BER(measure_count) = BER

measure_count < 3

N

Y

Report

BER(0:3) and offset(0:3)

END

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6. Conclusion

Implemented the BIST logic.

→ Examine the t, V margins using the stereographic BER diagram.

Using the bit error model,

→ Linear relationship between $1/\sqrt{|Log_{10}(BER)|}$ **and timing margin**

Suggest the sequence of accelerated measurement using the linear fitting .

The entire test is completed within 8~9 measurements for BER of 10^{-8} **to** 10^{-9}**.**

→ The BER test down to 10^{-15} **at 1Gbps can be finished within 150msec.**

Under the these circumstance, I will keep finding more precisely modeling .

References

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