

NESEA 2011 Program

Welcome Reception - 7th December
18:00-20:00pm - Park View Room
DAY 1 - 8th December
08:00-09:00 - On-Site Registration
09:00-09:15 - Conference Opening - Dr. Kevin Lee
09:15-10:15 - Keynote Speech: Baden Hughes, Event Zero (Chair: Danny Hughes)
10:15-10:30 - Tea and Coffee Break - Admiralty Gulf Room
10:30-12:00 - NESEA - SESSION 1 - Chair: Kevin Lee
<p>Jae-Hyun Jun, Hyunju Oh and Sung-Ho Kim DDoS flooding attack detection through a step-by-step investigation</p> <p>Danny Hughes, Wouter Horre, Binbin Qian, Tianlin Yu, Haofan Zhang and Zhun Shen. On the Problem of Implicit Dependencies in Contemporary Component Models</p> <p>Suryaprasad Jayadevappa, Praveen Kumar, Roopa D and Arjun A K. A Novel Low-Cost Intelligent Shopping Cart</p>
12:00-13:30 - Lunch - Atrium Garden Restaurant
13:30-15:00 - NESEA - SESSION 2 - Chair: Suryaprasad Jayadevappa
<p>Zhi-Bin Yu, Yong-Do Choi, Gi-Beom Kil and Sung-Ho Kim. Traffic Classification based on Visualization</p> <p>Delano Medeiros Beder, Jo Ueyama and Marcos L. Chaim, A Generic Policy-free Framework for Fault-tolerant Systems: Experiments on WSNs</p> <p>Fahime Farahnakian, Masoumeh Ebrahimi, Masoud Daneshtalab, Pasi Liljeberg and Juha Plosila. Q-learning based Congestion-aware Routing Algorithm for On-Chip Network</p>
15:00-15:30 - Tea and Coffee Break - Admiralty Gulf Room
15:30-16:30 - NESEA - SESSION 3 - Chair: Danny Hughes
<p>Maryam Kamali, Luigia Petre, Kaisa Sere and Masoud Daneshtalab. CorreComm: A Formal Hierarchical Framework for Communication Designs</p> <p>Eunkyun In, Jongju Park, Sangwoo Ahn, Cheoljon Jang and Jongwha Chong. Design of One chip Communication Stack Processor and MMS Communication Stack Library Based on IEC 61850</p>
17:30 - Social Event: Swan River Cruise and Dinner - leaving from Esplanade Hotel
DAY 2 - 9th December
08:00-09:00 - On-Site Registration
09:00-10:30 - NESEA - SESSION 4 - Chair: Heider Marconi
<p>Hyuk-In Kwon, Rize Jin and Tae-Sun Chung. AB-FTL: An Alternative Block Flash Translation Layer Using Locality-Aware Technique</p> <p>Fatemeh Karami H. and Ali K. Horestani. New Structure for Adder with Improved Speed, Area and Power</p> <p>Reza Faghieh Mirzaee and Mohammad Eshghi. Design of an ASIP IDEA Crypto Processor</p>
10:30-11:00 - Tea and Coffee Break - Admiralty Gulf Room

11:00-12:30 DATICS Workshop – SESSION 1 –Chair: Danny Hughes

Shan-Jung Miao and Yarsun Hsu
Group Allocation: A Novel Fairness Mechanism for On-Chip Network

Hung-Jen Sun and Yarsun Hsu
Implementation and Analysis of Speculative Flow Control for On-chip Interconnection Network

Heider Marconi Guedes Madureira, Gilmar Silva Beserra, José Edil Guimarães De Medeiros and José Camargo Da Costa
System-Level Power Consumption Modeling Of A SOC For WSN Applications

12:30-13:30 – Lunch - Atrium Garden Restaurant

13:30-15:00 - DATICS Workshop – SESSION 2 – Chair: Kevin Lee

Boguslaw Cyganek
Adding Parallelism to the Hybrid Image Processing Library in Multi-Threading and Multi-Core Systems

Chi-Hoon Shin, Myeong-Hoon Oh, Sung Nam Kim and Seong Woon Kim
Fine-grained Power Gating of Datapath using FSM

Seong-Won Kang, Kee-Won Kwon and Jung-Hoon Chun
A Study on Accelerated Built-in Self Test of Multi-Gb/s High Speed Interfaces

15:00-15:30 – Coffee Break – Admiralty Gulf Room

16:00-16:30 – Conference Closing and Best Paper Awards – Dr. Danny Hughes